REMARKS

Claims 1 - 19 are pending and under consideration. Claims 1, 7, 10 and 17 have been amended to clarify the claimed invention.

In the Office Action of January 22, 2003, claims 1 - 19 were rejected as being unpatentable over Watanabe et al.[1] in view of Fujiwara et al.[2] under §103(a)[3]. Applicants respectfully disagree and submit that claims 1-19 are patentable.

In particular, each of the independent claims (claims 1, 7, 10, 17) includes the limitation that the variable length coding of a second data block begins after the end of variable length coding of a first data block. This is not fairly taught or suggested in the cited art.

The Examiner asserts that this feature is taught by Fujiwara. Specifically, the Examiner cites to col. 8, lines 27-36 of the Fujiwara specification, which states:

> The decoding circuit in FIG. 1 may be arranged such that, upon completion of initializing a first block, the initializing address generating circuit 127 supplied a write request signal to the address adder 119, and that, until the address adder 119 receives this write request signal, the address adder 119 waits without inverting the first and second selection signals respectively on the signal lines 120a and 120b and gives a wait signal to the VLD 101, even though the address adder 119 has received the EOB detection signal on the signal line 104.

However, this portion of the Fujiwara specification goes on to explain, "According to this arrangement, writing a third block never starts before reading and initializing the first block and writing a second block are completed. To increase the speed of reading and initializing blocks in the first and second scan transform RAM 131a, 131b, it is effective, for example, to execute the reading and initializing per a plurality of data words." (Fujiwara at col. 8, lns. 36-42). Applicants respectfully submit that this does not teach the limitation that the variable length coding of a second data block begins after the end of variable length coding of a first data block.

First, Fujiwara appears to teach that the variable length coding of a second block does not begin after the end of variable length coding of a first block, but rather, "writing a third block *never starts before* reading and initializing the first block and writing a second block are completed."

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[1] U.S. Pat. No. 5,675,331.
[2] U.S. Pat. No. 5,689,254.
[3] 35 U.S.C. §103(a).

Second, Fujiwara does not teach parallel processing of variable length coding, and the wait operation disclosed in Fujiwara (col. 8, ln. 32) does not control the order of variable length coding in parallel processing.

Accordingly, Fujiwara does not provide any suggestion or motivation to one of skill in the art to use the inventor's particular method of variable length coding in parallel processing.

Further, the foregoing features are nowhere taught or fairly suggested by Allen et al., or the combination of Fujiwara et al. and Watanabe et al. In fact, as explained above, Fujiwara actually teaches away from the limitation that the variable length coding of a second data block begins after the end of variable length coding of a first data block. Accordingly, this limitation distinguishes the independent claims over the cited prior art.

Pending claims 2 - 6, 8 - 9, 11 - 16 and 18 - 19 are dependent claims that depend from independent claims 1, 7, 10 and 17 respectively. Because the independent claims are patentable over the cited art as discussed above, the dependent claims are likewise patentable over the cited references because they incorporate the limitations of their respective independent claim.

CONCLUSION

In view of the foregoing, Applicants respectfully submit that pending claims 1 – 19 are patentable. Further, all of the Examiner's objections and rejections have been addressed herein. It is, therefore, submitted that the application is in condition for allowance.

Notice to that effect is respectfully requested.

Respectfully submitted,
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail with the United States Postal Service with sufficient postage in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 13, 2003.

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